Reg. No. :

Question Paper Code : 70783

M.C.A. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

First Semester

MC5101 – COMPUTER ORGANIZATION

(Regulations 2017)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. State absorption law.
2. Find the binary equivalent of the given hexadecimal number A052.
3. Name a gate which can simulate a comparator. What are the comparisons performed by it ?
4. List two applications of decoders.
5. What is a normalized floating point number ? How is it stored in IEEE standard ?
6. What is program counter ? How does it sequence instruction execution ?
7. What is operand forwarding ?
8. Give two examples for control hazard.
9. Draw a block schematic of I/O connected as a daisy chain.
10. Define cache miss.

PART – B (5×13=65 Marks)

11. a) i) Draw the logic circuit using two input NAND gate to implement the following function : F(A, B, C, D) = (A ⊕ B)′ + AB. (3)

ii) Find the simplest sum of products form of the function using Quine McClusky method f = wxyz′ + wxy′z + w′xyz′ + wx′yz′ + wxyz. (10)

(OR)

b) i) Draw a multiple level NOR circuit for the following expression : AB′E + CD′E + BC. (3)

ii) Simplify the following two function using K-map :

- $F = \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + ABC\bar{D} + \bar{A}BCD + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}CD$
- F(w, x, y, z) = πM(2, 3, 5, 5, 7, 8, 12, 14). (10)

12. a) i) Design and implement a mod-4 counter that occurs in the following repeated sequence 000-->010-->011-->100-->000 using JK FF. (10)

ii) Mention the State diagram, State table and State equation. (3)

(OR)

b) i) State the significance of a high priority encoder. (3)

ii) Design a full subtractor using 2 × 4 decoder and appropriate gates. (10)

13. a) i) Explain the instruction set architecture and also discuss the different addressing modes. (10)

ii) Describe the floating point representation that uses excess 127 format. (3)

(OR)

b) Draw the block schematic for floating point operation and explain arithmetic operation for floating point numbers. (13)

14. a) Explain the different hazards in pipe lined processor with examples. (13)

(OR)

b) Consider a single data path processor and explain the sequence of control signal involved in executing ADD R1, R2 instruction. (13)

15. a) Discuss the cache block replacement policy of FIFO, LRU and MRU for a cache implemented with direct mapping scheme. Compare the policy in terms of miss rate. (13)

(OR)

b) Draw and explain the block diagram of DMA controller and also discuss the different bus arbitration approaches in DMA. (13)

70783

PART – C (1×15=15 Marks)

16. a) i) Design a comparator circuit which accepts 2 bit input (A_1, A_0 and B_1 B_0) and performs addition, if the inputs are equal otherwise performs subtraction. (10)

ii) Draw the circuit diagram of ring counter. (5)

(OR)

b) i) Design an ALU circuit which perform addition and subtraction only. (5)

ii) The 4-bit shift register is enclosed in one IC package. Draw the block diagram of the IC showing all inputs, outputs and connection by implementing the following function able. (10)

Function Table

Mode Control		Register Operation
S1	S0	
0	0	Complement input
0	1	No change
1	0	Left shift
1	1	Right shift