Reg. No. :

Question Paper Code : 90178

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019
Third/Fourth Semester
Electronics and Communication Engineering
EC 8392 – DIGITAL ELECTRONICS
(Common to Medical Electronics/Biomedical Engineering/Computer and Communication Engineering/Mechatronics Engineering/Robotics and Automation Engineering)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. State De-Morgan's theorem and mention its use.
2. Convert decimal 8723 to both BCD and ASCII codes. For ASCII an even parity bit is to be appended at the left.
3. Convert a two-to-four line decoder with enable input to 1 : 4 demultiplexer.
4. Implement Full adder using two half adder.
5. Construct a T Flip-flop from a D Flip-flop.
6. What is the difference between Mealy and Moore state machines ?
7. Distinguish between fundamental mode asynchronous sequential circuit and pulse mode asynchronous sequential circuits.
8. What is called dynamic hazard in asynchronous sequential circuit ?
9. Explain fan-in and fan-out of a standard TTL IC.
10. What is programmable logic array ? How it differs from ROM ?

PART – B (5×13=65 Marks)

11. a) Simplify the following using Quine Mc-Clusky method.

F(A, B, C, D) = Σ(0, 1, 2, 3, 5, 7, 8, 10, 12, 13, 15) (13)

(OR)

b) i) Given F(A, B, C, D)= ∏(1, 3, 6, 9, 11, 12, 14), draw the K-Map and obtain the simplified expression. (6)

ii) Simplify and implement F(A, B, C, D) = Σ(0, 4, 8, 9, 10, 11, 12, 14) using only NOR-OR logic. (7)

12. a) Explain the operation of BCD to Excess three code Converter. (13)

(OR)

b) i) Explain 4-bit magnitude comparator with three outputs: A > B, A = B and A < B. (8)

ii) Explain the operation of two bit binary multiplier in detail. (5)

13. a) Design a sequential circuit which has three flip flops A, B and C ; one input X_ in ; and one output Y_out. The state diagram is shown in Figure 1. The circuit is to be designed by treating the unused states as don't care conditions. Analyze the circuit obtain from the design to determine the effect of the unused states. Use D flip flops in the design. (13)

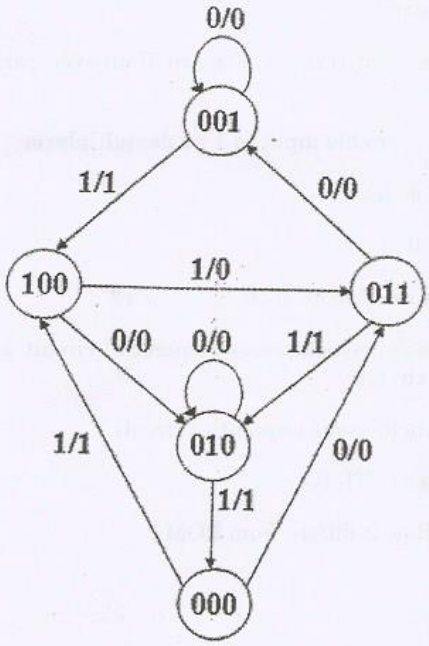

Figure 1

(OR)

90178

b) i) Design a BCD synchronous counter which counts in the sequence.

0000,0001,0010,0011,0100,0101,0110,0111,1000,1001,0000 **(10)**

ii) Discuss the working of 4 bit Johnson Counter with neat diagram. **(3)**

14. a) An asynchronous sequential circuit is described by the following excitation and output function.

$Y = X_1X_2' + (X_1 + X_2')\,Y$, $Z = Y$.

i) Draw the logic diagram. **(3)**

ii) Derive the transition table and output map. **(5)**

iii) Describe the behavior of the circuit. **(5)**

(OR)

b) i) Discuss in detail about Races. **(6)**

ii) Explain the race free state assignment. **(7)**

15. a) i) Implement the following using PLA. **(6)**

F1 = A'B + AC' + A'BC'

F2 = (AB + AC + BC)'

ii) Explain TTL log logic family with totem pole output. **(7)**

(OR)

b) i) State the advantages of CMOS logic circuit. **(3)**

ii) Explain static RAM cell using MOSFET. **(3)**

iii) Write a notes on FPGA with neat diagram. **(7)**

PART – C **(1×15=15 Marks)**

16. a) i) Design an odd parity generator that generates an odd parity bit for every input string of 3 bits. **(10)**

ii) Explain the need of Parity Checker circuit with necessary diagrams. **(5)**

(OR)

b) Derive the state table and state diagram of the sequential circuit shown in figure. Explain the function that the circuit performs. **(15)**