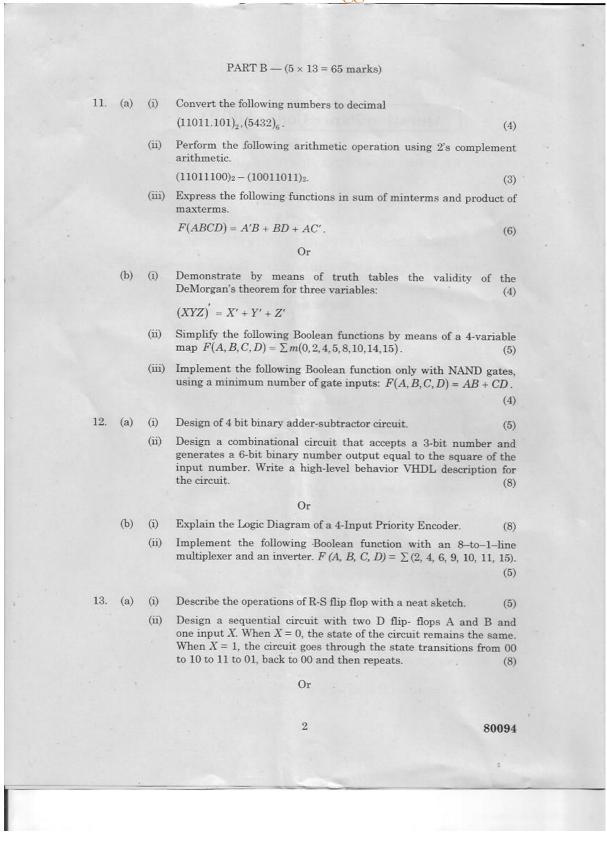
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	Question Paper Code: 80094
	B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.
	Third Semester
	Computer Science and Engineering
	CS 8351 - DIGITAL PRINCIPLES AND SYSTEM DESIGN (Common to Electronics and Telecommunication Engineering/Information
	Technology)
	(Regulation 2017)
Tim	e: Three hours Maximum: 100 marks
	Answer ALL questions. $PART A - (10 \times 2 = 20 \text{ marks})$
1.	Represent 3856 in BCD and 2421 code.
2.	Simplify the following Boolean function.
	F = x'y' + xy + x'y.
0	
3.	Construct a full adder using two half adders and OR gate.
4.	Write the truth table of 2 to 4 line decoder and draw its logic diagram.
5.	State the difference between latches and flipflops.
6.	What is meant by edge triggered flip flops?
7.	Draw the logic diagram and write the function table of D Latch.
8.	What is meant by race free condition in sequential circuits?
9.	What are error detecting codes? Give examples.
10.	List the advantages of using sequential programmable devices.

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		(b)	(i)	Construct a clocked Master Slave J-K Flip flop and explain.	(5)
			(ii)	A sequential circuit with two D flip-flops A and B, two inputs X a	nd
				Y, and one output Z is specified by the following input equations:	(8)
				A(t+1) = x'y + xA	
				B(t+1) = x'B + xA $z = B$	
				Draw the logic diagram of the circuit. Derive the state table a state diagram and state whether it is a Mealy or a Moore machine	nd
	14.	(a)	(i)	Write the difference between synchronous and asynchronous	
			(ii)	Outline the procedure for analyzing asynchronous sequent	2.0
				Or	
		(b)	(i)	Discuss about the possible hazards and methods to avoid them combinational circuits.	in (5)
			(ii)	Discuss about the possible hazards in sequential circuits.	(8)
	15.	(a)	(i)	Discuss briefly about RAM and its types.	(5)
			(ii)	Explain the logical construction of a 256×8 RAM using 64×8 RA chips.	M (8)
				Or	
		(b)	(i)	Given the 8 bit data word 10011010 generate the 13 bit composition word for the Hamming code that corrects single errors and detection double errors.	ect
			(ii)	T-1 th cu	(4) (9)
				F1(A, B, C) = AB' + AC + A'BC'	9)
				F2(A,B,C) = (AC + BC)'.	
				PART C — (1 × 15 = 15 marks)	
	16.	(a)	(i)	Design a BCD to excess-3 code converter and explain.	(8)
			(ii)	Draw and explain the logic circuit of a 4-bit magnitude comparato	r. (7)
				Or	
		(p)	(i)	Explain the operations of a 4-bit bidirectional Shift Register.	(8)
			(ii)	Write the VHDL code for a 4-bit binary -up counter and explain.	(7)
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