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B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2012.

Fourth Semester

Computer Science and Engineering

CS 2253/141403/CS 43/CS 1252 A/10144 CS 404/080250011 — COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is SPEC? Specify the formula for SPFC rating.
2. What is relative addressing mode? When is it used?
3. Write the register transfer sequence for storing a word in memory.
4. What is hard-wired control? How is it different from micro-programmed control?
5. What is meant by data and control hazards in pipelining?
6. What is meant by speculative execution?
7. What is meant by an interleaved memory?
8. An address space is specified by 24 bits and the corresponding memory space by 16 bits:

   How many words are there in the
   (a) virtual memory
   (b) main memory.
9. Specify the different I/O transfer mechanisms available.
10. What does isochronous data stream means?

PART B — (5 × 16 = 80 marks)

11. (a) (i) What are addressing modes? Explain the various addressing modes with examples. (8)

(ii) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. (8)

Or

(b) (i) Explain instruction sequencing in detail. (10)

(ii) Differentiate RISC and CISC architectures. (6)

12. (a) (i) With a neat diagram explain the internal organization of a processor. (6)

(ii) Explain how control signals are generated using microprogrammed control. (10)

Or

(b) (i) Explain the use of multiple-bus organization for executing a three- operand instruction. (8)

(ii) Explain the design of hardwired control unit. (8)

13. (a) (i) Discuss the basic concepts of pipelining. (8)

(ii) Describe the data path and control considerations for pipelining. (8)

Or

(b) Describe the techniques for handling data and instruction hazards in pipelining. (16)

14. (a) (i) Explain synchronous DRAM technology in detail. (8)

(ii) In a cache-based memory system using FIFO for cache page replacement, it is found that the cache hit ratio H is low. The following proposals are made for increasing.

(1) Increase the cache page size

(2) Increase the cache storage capacity

(3) Increase the main memory capacity

(4) Replace the FIFO replacement policy by LRU.

Analyze each proposal to determine its probable impact on H. (8)

Or

(b) (i) Explain the various mapping techniques associated with cache memories. (10)

(ii) Explain a method of translating virtual address to physical address. (6)

15. (a) Explain the following :

(i) Interrupt priority schemes (8)

(ii) DMA. (8)

Or

(b) Write an elaborated note on PCI, SCSI and USB bus standards. (16)
