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Question Paper Code : 21393

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulations 2008/2010)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is named dependence?

2. Prediction accuracy is 80%(for instruction in the buffer). Hit rate in the buffer is 90% (for branch prediction taken). Compute the branch penalty.

3. List any five primary characteristics of EPIC multiple issue processor.

4. What are the limitations of multiple issue processor?

5. Give the taxonomy of Parallel architecture.

6. Suppose you want to achieve a speed up of 90 with 100 processors. What fraction of the original computation can be sequential?

7. A certain memory configuration has four levels M_1, M_2, M_3 and M_4 with hit ratios of 0.7, 0.85, 0.97, 1.0 respectively. A program P makes 3000 references to this memory system. Calculate the exact number of references Ri made by P to each level of memory, Mi.

8. Compare static and dynamic RAM.

9. What is multi core microprocessor? Give its advantages.

10. What is CMP? List the features of CMP.

PART B — (5 × 16 = 80 marks)

11. (a) (i) With a neat diagram explain the Tomasulo-based processor. (10)

(ii) Briefly explain the dynamic branch prediction techniques. (6)

Or

(b) (i) Consider the following code and assume that the multiply instruction has a latency of 5, the divide instruction a latency of 10 and the add instruction latency is 2. Also assume that there are separate functional units for effective address calculations, for ALU operations, and for branch condition evaluation. For a Speculative processor, create a table showing when each instruction issues, executes, write the result and commits, for one iteration of the loop and for atleast two instructions from the second iteration. Assume one CDB and that only one instruction can commit per cycle. (10)

```
Loop :  LD F0, 0(R1)
        LD F4, 0(R2)
        ADD F0, F0, F2
        MUL F4, F4, F2
        DIV F0, F0, F4
        SD 0(R2), F0
        ADDI R1, R1, #8
        ADDI R2, R2, #8
        SUBI R3, R3, #1
        BNEZ R3, loop
```

(ii) Discuss the basic compiler techniques for exposing ILP. (6)

12. (a) Explain the VLIW approach with example. (16)

Or

(b) (i) Give the limitations of ILP. (6)

(ii) Discuss the major advantages and disadvantages of supporting speculation in software and hardware. (10)

13. (a) Give the symmetric shared memory architecture. Also explain the basic schemes for enforcing cache coherence. (16)

Or

(b) (i) Explain the relaxed consistency model. (8)

(ii) Assume that words X_1 and X_2 are in the same cache block, which is in the shared state in the caches of both P_1 and P_2. Assuming the following sequence of events, identify each miss as a true sharing miss, a false sharing miss, or a hit. Any miss that would occur if the block size were one word is designated a true sharing miss. (8)

Time	P_1	P_2
1	Write X_1	
2		Read X_2
3	Write X_1	
4		Write X_2
5	Read X_2	

14. (a) Discuss the various cache Optimization techniques. (16)

Or

(b) (i) Briefly describe the various RAID levels. (8)

(ii) Explain the steps in designing an I/O system. (8)

15. (a) (i) Discuss the design challenges in SMT. (8)

(ii) Write short notes on heterogeneous multicore processors. (8)

Or

(b) With a neat diagram explain the Intel Multicore architecture. (16)