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B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2012.

Third Semester

Computer Science and Engineering

CS 2202/141302/CS 34/EC 1206 A/10144 CS 303/080230012 — DIGITAL PRINCIPLES AND SYSTEMS DESIGN

(Common to Information Technology)

(Regulation 2008)

(Common to PTCS 2202 – Digital Principles and Systems Design for B.E. (Part-Time) Second Semester – CSE – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Realise OR gate using only NAND gates.
2. Find the complement and dual of $F = x(y'z' + yz)$.
3. Implement a full adder with two half adders.
4. Implement a 4-bit even parity checker.
5. Construct a 4 × 16 decoder using 3 × 8 decoders.
6. What is a combinational PLD?
7. List any two mechanisms to achieve edge triggering of flip flops.
8. What is a ring counter?
9. Distinguish between a conventional flow chart and an ASM chart.
10. Draw the block diagram of an asynchronous sequential circuit.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify F(A, B, C, D) = Σ(0, 1, 2, 5, 8, 9, 10) in sum of products and product of sums using K-map. (12)

(ii) Write notes on negative and positive logic. (4)

Or

(b) (i) Simplify the expression F(A, B, C, D) = Σ (1, 4, 6, 7, 8, 9, 10, 11, 15) using Quine-McClusky method. (12)

(ii) Check if NOR operator is associative. (4)

12. (a) (i) Analyse the combinational circuit shown in figure 12 (a) (i) to determine the truth table and the Boolean expressions governing the outputs of the circuit. (10)

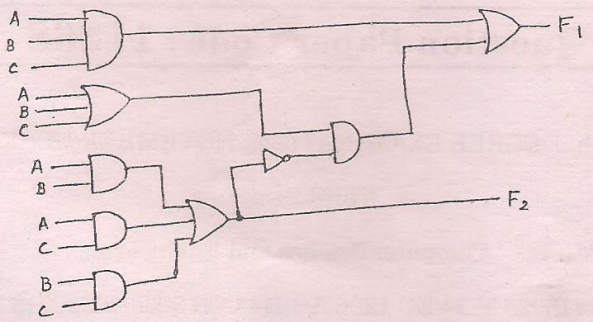

Figure 12 (a) (i)

(ii) Explain BCD adder with a neat block diagram. (6)

Or

(b) (i) Design a BCD to excess-3 code converter using logic gates. (12)

(ii) Draw the diagram of a 4-bit adder subtractor using full adders. (4)

13. (a) (i) Write notes on PLA and PAL. (8)

(ii) Implement F(A, B, C, D) = $\Sigma(1, 3, 4, 11, 12, 13, 14, 15)$ using 8×1 multiplexer. (8)

Or

(b) (i) Write notes on RAM, its operations and its types. (10)

(ii) Design a 4-input priority encoder. (6)

14. (a) (i) Design a 3-bit binary counter. (10)

(ii) Write the HDL description of T flip flop and JK flip flop from D flip flop and gates. (6)

Or

(b) Design a sequential circuit using RS flip flops for the state table given below using minimum number of flip flops. (16)

Present state	Next state		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

15. (a) Explain race-free state assignment with an example. (16)

Or

(b) Write detailed notes on hazards in combinational circuits and sequential circuits. (16)

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