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Question Paper Code : 21363

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Fifth Semester

Electronics and Communication Engineering

EC 2303 / EC 53 / 10144 EC 605 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulation 2008/2010)

(Common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester, Electronics and Communication Engineering, Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write any two types of instruction.
2. Let X = 1010100 and Y = 1000011. Perform
   (a) X-Y and
   (b) Y-X using 2's complement.
3. What is a carry look ahead adder?
4. What is coprocessor and what functions are performed by the coprocessor?
5. Define pipeline speedup and efficiency.
6. What is superscalar processing?
7. What are the differences between asynchronous and synchronous DRAM?
8. What is content addressable memory and what are advantages of this memory?
9. Differentiate between RISC and CISC architecture.
10. Why does DMA have priority over the CPU when both request a memory transfer?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Describe the general approach for register-level systems design with an example. (8)

(ii) Derive a state table for a synchronous sequential circuit that acts as a serial incrementer. An unsigned number N of arbitrary length is entered serially on input line x, causing the circuit to output serially the number N+1 on its output line z. (8)

Or

(b) (i) Briefly explain various addressing modes in detail. (10)

(ii) What is a multiplexer? Explain the realization of two-input, 4-bit-multiplexer at gate-level. (6)

12. (a) (i) Design a 4-bit adder-subtractor circuit using full adder and explain. (8)

(ii) Illustrate non-restoring division algorithm with an example. (8)

Or

(b) (i) Explain the IEEE standard for floating-point numbers in detail. (8)

(ii) Design a 16-bit-carry-lookahead adder using 4-bit adders and explain. (8)

13. (a) (i) Describe the organization of a typical microprogrammed control unit organization with the help of a diagram. (8)

(ii) What is an instruction pipeline? Describe the organization of a four-stage pipeline with the help of diagram. (8)

Or

(b) (i) Describe the structure of a typical microprogram sequencer in detail. (8)

(ii) Describe any two techniques for dealing data dependencies in pipelined computers. (8)

14. (a) (i) Describe the optical readout mechanism for a CD-ROM with the help of diagram. (8)

(ii) Explain how virtual address is translated into real address in segmented memory system. (8)

Or

(b) (i) Explain preemptive and non-preemptive memory allocation strategies in detail. (8)

(ii) Briefly compare the mapping procedures used in cache memory organization. (8)

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (8)

(ii) What are handshaking signals? Explain asynchronous data transfer using handshake signals. (8)

Or

(b) (i) What is bus arbitration? Describe the centralized approach for bus arbitration with the help of diagram. (8)

(ii) Describe the architecture of a typical superscalar processor with the help of a block diagram. (8)

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