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Question Paper Code : 71444

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 — DIGITAL ELECTRONICS

(Regulation 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester –
Electronics and Communication Engineering Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define 'min term' and 'max term'.
2. Write a note on tristate gates.
3. Give the logic expressions for sum and carry in full adder circuit.
4. Give examples for combinational circuit (any four).
5. Realize T FF and JK FF.
6. Draw the circuit diagram of a 3 bit Ring counter.
7. Compare static and dynamic RAM cell (any two).
8. $Y = A\bar{B} + \bar{A}$. Implement using ROM.
9. Differentiate flow chart and ASM chart.
10. List the problems that arise in asynchronous circuits.



PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify $T(x, y, z) = (x + y) [\overline{x(y + z)}] + \overline{x} \overline{y} + \overline{x} \overline{z}$. (6)
- (ii) Simplify the Boolean function and draw the logic diagram $f(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (10)

Or

- (b) (i) Realize AND, OR and NOT gates using NAND gate. (6)
- (ii) Using tabulation method simplify $F(A, B, C, D, E) = \Sigma(0, 1, 4, 5, 16, 17, 21, 25, 29)$. (10)

12. (a) Design a combinational circuit that converts 4 bit Gray Code to a 4 bit binary number. Implement the circuit.

Or

- (b) Detail the following :
- (i) BCD adder. (8)
- (ii) Magnitude comparator. (8)

13. (a) (i) Describe a JK FF with its characteristic table and characteristic equation. (6)
- (ii) With a neat sketch describe a 3 bit synchronous up/down counter. Draw the timing waveform. (10)

Or

- (b) Design a sequential circuit with two D FFs A and B and one input x . When $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from 00 - 01 - 11 - 10 - 00 - 01...

14. (a) (i) List the steps involved in memory read and memory write operations. (10)
- (ii) Give an account for classification of memories. (6)

Or

- (b) Explain the structure of PAL and PLA. How a combinational logic function is implemented in PAL and PLA? Explain with an example for each. (16)

15. (a) (i) Write the VERILOG code for full adder and JK FF. (8)
- (ii) Explain the different types of hazards. Design a hazard free circuit for $y = x_1 x_2 + x_2' x_3$. (8)

Or

- (b) With ASM chart design a binary multiplier. (16)