

VL5008 SELECTED TOPICS IN ASIC DESIGN

DETAILED SYLLBUS

OBJECTIVES:

- The course focuses on the semi-custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICs, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS

Anti-fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECTURE

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V HIGH PERFORMANCE ALGORITHMS FOR ASICs/ SOCS. SOC CASE STUDIES

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

REFERENCES:

1. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
2. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
3. M. J. S. Smith, " Application - Specific Integrated Circuits", Pearson,2003
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, "FPGA-based Implementation of Signal Processing Systems", Wiley, 2008
6. Steve Kilts, "Advanced FPGA Design," Wiley Inter-Science.