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For Questions, Notes, Syllabus & Results

AP5094 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

DETAILED SYLLABUS

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance, wave propagation, reflection, and bounce diagrams Reactive terminations – L, C, static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stack ups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and strip line Reflection and terminations for logic gates, fanout, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk, minimizing cross-talk (strip line and microstrip) Differential signalling, termination, balanced circuits, S-parameters, Lossy and Loss les models

UNIT III NON-IDEAL EFFECTS

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, $tan\delta$, routing parasitic, Common-mode current, differential-mode current, Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN

SSN/SSO, DC power bus design, layer stack up, SMT decoupling, Logic families, power consumption, and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Bit streams, PRBS and filtering functions of link-path components, Eye diagrams, jitter, inter-symbol interference Bit-error rate, Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, cancelling parasitic capacitance, Clock jitter.

REFERENCES:

- 1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003.
- 2. Eric Bogatin, Signal Integrity Simplified, Prentice Hall PTR, 2003.
- 3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
- 4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Inter science, 2000.