VL5202 LOW POWER VLSI DESIGN

DETAILED SYLLABUS

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques for Leakage Power Reduction - Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-Bi CMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random-access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION

Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER

Synthesis for low power – Behavioral level transform – software design for low power.

REFERENCES

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2. A. P. Chandrasekaran and R. W. Broadersen, “Low power digital CMOS design”, Kluwer,1995.

3. Dimitrios Soudris, C. Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power” Kluwer, 2002.

4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

5. James B. Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.

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7. Kaushik Roy and S. C. Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.

8. Kiat -send Yeo, Kaushik Roy “Low-Voltage, Low-power VLSI Subsystem”, Tata McGraw-Hill, 2009