

## **VL5291 VLSI SIGNAL PROCESSING**

### DETAILED SYLLABUS

#### **OBJECTIVES:**

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

#### **UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

#### **UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

#### **UNIT III ALGORITHMIC STRENGTH REDUCTION -II**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

#### **UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

#### **UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

#### **REFERENCES:**

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Inter science, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.