VL5201 TESTING OF VLSI CIRCUITS

DETAILED SYLLABUS

OBJECTIVES:

The students should be made to:

- Understand logic fault models
- Learn test generation for sequential and combinational logic circuits

UNIT I TESTING AND FAULT MODELLING

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY

Design for Testability – Ad-hoc design – generic scan-based design – classical scan-based design– system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

REFERENCES:

1. A. L. Crouch, “Design Test for Digital IC"s and Embedded Core Systems”, Prentice Hall International, 2002.

2. M. Abramovici, M. A. Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.

3. M. L. Bushnell and V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory And Mixed Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.

4. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.