VL5191 DSP INTEGRATED CIRCUITS

DETAILED SYLLABUS

OBJECTIVES:

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multi rate systems and finite word length effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects – Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III DSP ARCHITECTURES

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks-Storage elements – clocking of synchronous systems, Asynchronous systems -FSM

UNIT V ARITHMETIC UNIT AND PROCESSING ELEMENTS

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

REFERENCES:

1. B. Venkatramani, M. Bhaskar, “Digital Signal Processors”, Tata McGraw-Hill, 2002.

2. John J. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Pearson Education, 2002.

3. Keshab Parhi, “VLSI Digital Signal Processing Systems design & Implementation”, John Wiley & Sons, 1999.

4. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York, 1999.