AP5301 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES

DETAILED SYLLABUS

OBJECTIVES:

- To familiarize about the features, specification and features of modern microprocessors.
- To gain knowledge about the architecture of Intel 32- and 64-bit microprocessors and salient features associated with them.
- To familiarize about the features, specification and features of modern microcontrollers.
- To gain knowledge about the 32-bit microcontrollers based on ARM and PIC32 architectures

UNIT I FEATURES OF MODERN MICROPROCESSORS

Evolution of microprocessors - Data and Address buses – clock speed – memory interface - multi-core architectures – cache memory hierarchy – operating modes – super scaler execution – dynamic execution – over clocking – integrated graphics processing - performance benchmarks.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURES

Introduction to IA 32-bit architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64-bit extension technology – Intel 64-bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE - ARM

RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3-stage pipeline ARM organization - 3-stage pipeline ARM organization – ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles)

UNIT IV FEATURES OF MODERN MICROPROCESSORS

Introduction to microcontrollers – microcontroller vs microprocessors – microcontroller architecture - Processor Core – Memory interfaces– Communication interfaces (SPI, I2C, USB and CAN) – ADC - PWM – Watchdog timers – Interrupts – Debugging interfaces

UNIT V HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cotex-M3 architecture

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1. Barry. B. Breg, "The Intel Microprocessors", PHI,2008.

2. Gene.H. Miller. "Micro Computer Engineering", Pearson Education, 2003.

3. Intel Inc, "Intel 64 and IA-32 Architectures Developer's Manual", Volume-I, 2016

4. Joseph Yiu, "The Definitive Guide to the ARM ® Cortex-M3", Newnes, 2010.

5. Scott Mueller, "Upgrading and Repairing PCs", 20th edition, Que.

6. Steve Furber, „" ARM System –On –Chip architecture "Addision Wesley, 2000.

7. Trevor Martin, "The Designer's Guide to the Cortex-M Processor Family", Newnes, 2013.