AP5006 PHYSICAL DESIGN OF VLSI CIRCUITS

DETAILED SYLLABUS

UNIT I INTRODUCTION TO VLSI TECHNOLOGY

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

OBJECTIVES:

To introduce the physical design concepts such as routing, placement, partitioning and packaging

To study the performance of circuits layout designs, compaction techniques.

REFERENCES:

1. Preas M. Lorenzatti, “Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.

2. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill Int. Edition 1995