AP5005 SYSTEM ON CHIP DESIGN

DETAILED SYLLABUS

UNIT I INTRODUCTION

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design

UNIT II SYSTEM LEVEL MODELLING

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples

UNIT III HARDWARE SOFTWARE CO-DESIGN

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV SYNTHESIS

System synthesis: Transaction Level Modelling (TLM) based design, automaticTLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling

UNIT V SOC VERIFICATION AND TESTING

SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism

OBJECTIVES:

Understanding of the concepts, issues, and process of designing highly integrated SoCs following systematic hardware/software co-design & co-verification principles

REFERENCES

1. D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004.

2. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009

3. Erik Larson, Introduction to advanced system-on-chip test design and optimisation, Springer 2005

4. Grotker, T., Liao, S., Martin, G. & Swan, S. System design with System C, Springer, 2002.

5. Ghenassia, F. Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems, Springer, 2010.

6. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, “Low power NoC for high performance SoCdesing”,CRC press, 2008.