AP5252 ASIC AND FPGA DESIGN **L T P C 3 0 0 3**

UNIT I OVERVIEW OF ASIC AND PLD 9

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II ASIC PHYSICAL DESIGN 9

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing – circuit extraction - DRC

UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV FIELD PROGRAMMABLE GATE ARRAYS 9

FPGA Design: FPGA Physical Design Tools -Technology mapping - Placement & routing – Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

UNIT V SOC DESIGN 9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching

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2. H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999

3. Jan. M. Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003

4. M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003

5. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.

6. P.K.Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.

7. Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008

8. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Pub.

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