AP5151 ADVANCED DIGITAL SYSTEM DESIGN

DETAILED SYLLABUS

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault table method-path sensitization method – Boolean difference method-D algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self-test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

REFERENCES:

1. Charles H. Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004

2. M. D. Ciletti, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.

3. M. G. Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.

4. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001

5. Parag K.Lala "Digital system Design using PLD" B S Publications,2003

6. Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002

7. S. Palnitkar, Verilog HDL – A Guide to Digital Design and Synthesis, Pearson, 2003.