EC8007 LOW POWER SoC DESIGN

DETAILED SYLLABUS

OBJECTIVES:

The student should be made to:

- Identify sources of power in an IC.
- Understand basic principle of System on Chip design
- Learn optimization of power in combinational and sequential logic machines for SoC Design
- Identify suitable techniques to reduce the power dissipation and design circuits with low power dissipation.

UNIT I POWER CONSUMPTION IN CMOS

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques for Leakage Power Reduction - Basic principle of low power design, Logic level power optimization – Circuit level low power design.

UNIT II SYSTEM-ON-CHIP DESIGN

System-on-Chip Concept, Design Principles in SoC Architecture, SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC

UNIT III POWER OPTIMIZATION OF COMBINATIONAL AND SEQUENTIAL LOGIC MACHINES FOR SOC

Introduction to Standard Cell-Based Layout – Simulation - Combinational Network Delay - Logic and interconnect Design - Power Optimization - Switch Logic Networks. Introduction - Latches and Flip-Flops - Sequential Systems and Clocking Disciplines - Sequential System Design - Power Optimization - Design Validation - Sequential Testing.

UNIT IV DESIGN OF LOW POWER CIRCUITS FOR SUB SYSTEM ON A SOC

Subsystem Design Principles - Combinational Shifters – Adders – ALUs – Multipliers – High Density Memory – Field Programmable Gate Arrays - Programmable Logic Arrays - Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random-access memories, low power clock, Inter connect and layout design

UNIT V FLOOR PLANNING

Floor-planning Methods – Block Placement & Channel Definition - Global Routing - switchbox Routing - Power Distribution - Clock Distributions - Floor-planning Tips - Design Validation - Off-Chip Connections – Packages, The I/O Architecture - PAD Design

TEXT BOOKS:

1. J. Rabaey, ―Low Power Design Essentials (Integrated Circuits and Systems) ‖, Springer, 2009

2. Wayne Wolf, ―Modern VLSI Design – System – on – Chip Design‖, Prentice Hall, 3rd Edition, 2008.

REFERENCES:

1. J.B. Kuo & J.H. Lou, ―Low-voltage CMOS VLSI Circuits‖, Wiley, 1999.

2. A. Bellaowar & M.I. Elmasry, ‖Low power Digital VLSI Design, Circuits and Systems‖, Kluwer, 1996.

3. Wayne Wolf, ―Modern VLSI Design – IP based Design‖, Prentice Hall, 4th Edition, 2008.

4. M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003

5. Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008

6. Recent literature in Low Power VLSI Circuits.

7. Recent literature in Design of ASICs