EC6019 DATA CONVERTERS

DETAILED SYLLABUS

OBJECTIVES:

- To explain the basic operational and design principles of CMOS Analog to Digital and Digital to Analog converter architectures.
- To introduce the design calculations for developing the various blocks associated with a typical CMOS AD or DA converter.
- To make students decide the dimensions and bias conditions of all the MOS transistors involved in the design.

UNIT I SAMPLE AND HOLD CIRCUITS

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION

Performance metrics, reference multiplication and division, switching and logic functions in AC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TEXT BOOK:

1. Behzad Razavi, “Principles of data conversion System Design”, IEEE press, 1995.

REFERENCES:

1. Franco Maloberti, “Data Converters”, Springer, 2007.

2. Rudy Van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters”, Kluwer Acedamic Publishers, Boston, 2003.