35241 – COMPUTER ARCHITECTURE

DETAILED SYLLABUS

UNIT I REGISTER TRANSFER LOGIC AND CPU

1.1 Register transfer: Register Transfer Language – Inter Register transfer – control function-Bus transfer-memory transfer

1.2 Micro operations and ALU: Arithmetic micro operations-Binary addersubtractor, incrementer, 4 bit arithmetic circuit, Logic micro operations- one stage of logic circuit applications, shift micro operations- 4 bit combinational circuit shifter-one stage of ALU

1.3 Central processing unit: components of CPU- General register organization, bus system-register set with common ALU-memory stack - stack limits, Instruction format(3,2,1,0 address instructions)

1.4 Control unit: structure of control unit-fetch cycle, indirect cycle, Execute cycle, interrupt cycle, instruction cycle.

UNIT II INPUT – OUTPUT MODULE

2.1 Input output Interface : Need for I/O interface, I/O bus and interface, I/O commands, Example of I/O interface

2.2 Asynchronous data transfer-strobe control, handshaking, Asynchronous serial transfer, Asynchronous communication interface

2.3 Modes of transfer- Programmed I/O,Interrupt initiated I/O-vectored interrupt, non vectored interrupt, Priority interrupt, Interrupt controller ,DMA –DMA controller, DMA transfer

2.4 I/O Processor: CPU-IOP communication. Serial communication

UNIT III MEMORY MODULE

3.1. Memory types: CPU registers, Main memory, Secondary memory, Cache 1Hr

3.2 Main Memory: ROM, RAM, Memory address map, memory connection to CPU

3.3 Secondary Memory: Magnetic tape , Magnetic Disk

3.4 Cache: Need for cache memory, operational principle, Cache initialization, Different mapping techniques, Writing into cache

3.5 Memory Management : Virtual memory concept-virtual address, physical address, memory table for mapping a virtual address, address mapping using pages, Associative memory page table, Page replacement technique

UNIT IV MICROPROCESSORS AND PARALLEL PROCESS

4.1 Microprocessor: Block diagram of 8086-registers: segment registers, address: effective address, flag registers and application of microprocessor

4.2 Parallel processing: types of parallel processing systems. Parallel organizations
4.3 Pipe Lining: instruction pipeline, arithmetic pipeline, pipelining in super scalar processors

UNIT V . ARCHITECTURE AND CONCEPTS OF ADVANCED PROCESSORS

5.1 Symmetric Multiprocessors: Organizations, a mainframe

5.2 Multithreading and clusters: Implicit and explicit multi threading, cluster configuration

5.3 NUMA and vector:: NUMA organizations and approaches to vector computation

5.4 Multi Core : Multicore organization

Text Book

1. COMPUTER SYSTEM ARCHITECTURE M.MORRIS MANO Prentice –Hall of India Pvt Limited THIRD EDITION

2. COMPUTER ORGANIZATION AND ARCHITECTURE designing for performance William Stallings Pearson Publications. Eighth Edition