34057- VERY LARGE SCALE INTEGRATION PRACTICAL

DETAILED SYLLABUS

LIST OF EXPERIMENTS

1. SIMULATION OF VHDL CODE FOR COMBINATIONAL CIRCUIT Optimize a 4 variable combinational function (SOP or POS), describe it in VHDL code and simulate it. Example: F= (0,5,8,9,12) in sop or pos
2. SIMULATION OF VHDL CODE FOR ARITHMETIC CIRCUITS Design and Develop the circuit for the following arithmetic function in VHDL Codes and Simulate it. Addition, Subtraction Multiplication (4 x 4 bits)
3. SIMULATION OF VHDL CODE FOR MULTIPLEXER Design and develop a 2 bit multiplexer and portmap the same for developing upto 8 bit multiplexer.
4. SIMULATION OF VHDL CODE FOR DEMULTIPLEXER Design and develop an 8 output demultiplexer. Simulate the same code in the software
5. VHDL IMPLEMENTATION OF MULTIPLEXER Describe the code for a multiplexer and implement it in FPGA kit in which switches are connected for select input and for data inputs a LED is connected to the output.
6. VHDL IMPLEMENTATION OF DEMULTIPLEXER Switches are connected for select inputs and a data input, Eight LEDs are connected to the output of the circuit.
7. VHDL IMPLEMENTATION OF 7 SEGMENT DECODER Develop Boolean expression for 4 input variables and 7 output variables. Design and develop a seven segment decoder in VHDL for 7 equations. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded to 7 segment equivalent.
8. VHDL IMPLEMENTATION OF 7 SEGMENT DECODER BY LUT Develop a 7 segment decoder using Look up table. Describe the seven segment decoder in VHDL using developed Look up table. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded into 7 segment equivalent.
9. VHDL IMPLEMENTATION OF ENCODER Design and develop HDL code for decimal (Octal) to BCD encoder. There will be10 input switches (or 8 switches) and 4 LEDs in the FPGA kit. The input given from switches and it is noted that any one of the switch is active. The binary equivalent for the corresponding input switch will be glowing in the LED as output.

10. SIMULATION OF VHDL CODE FOR DELAY Develop a VHDL code for making a delayed output for 1second or 2 seconds by assuming clock frequency provided in the FPGA Kit.
11. VHDL IMPLEMENTATION FOR BLINKING A LED Develop a VHDL Code for delay and verify by simulating it. This delay output is connected to LED. Delay is adjusted such away LED blinks for every 1 or 2 seconds.
12. SIMULATE A VHDL TEST BENCH CODE FOR TESTING A GATE Develop a VHDL test bench code for testing any one of the simple gate. Simulate the test bench code in the HDL software.
13. VHDL IMPLEMENTATION FOR BLINKING A ARRAY OF LEDS Design and develop a VHDL Code for 4 bit binary up counter. Four LEDs are connected at the output of the counter. The counter should up for every one seconds.
14. VHDL IMPLEMENTATION OF A SPELLER WITH AN ARRAY OF LEDS Design and develop VHDL Code for a 5 bit Johnson ring counter 4 bit The LEDs are connected at the output of the counter. The speller should work for every one seconds.
15. VHDL IMPLEMENTATION OF 7 SEGMENT DISPLAY Design and develop a seven segment decoder in VHDL. Design and develop a 4 bit BCD counter, the output of the counter is given to seven segment decoder. A seven segment display is connected to the output of the decoder. The display shows 0,1, 2.. 9 for every one second.